AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

Listing of Claims:

1. (Cancelled).

2. (Currently Amended) A semiconductor device comprising:

a semiconductor chip,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer and connected to said electrodes, and

external terminals provided on said circuit layer, wherein

an organic protecting film is provided on the plane opposite to said stress relaxing layer of said semiconductor chip,

said porous stress relaxing layer has a greater porosity than that of the organic protecting film, and

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed to outside of the semiconductor device on a same plane.

3. (Currently Amended) A semiconductor device comprising:

a semiconductor chip,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes of said semiconductor chip are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer,

via-holes provided between the electrodes on said semiconductor chip and said circuit layer,

conductive portions for connecting electrically said circuit layer and said electrodes in said via-holes,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane opposite to the plane where the circuits and electrodes of said semiconductor chip are formed, wherein

said porous stress relaxing layer has a greater porosity than that of the organic protecting film, and

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed to outside of the semiconductor device on a same plane.

4. (Previously Presented) A semiconductor device as claimed in claim 2 or 3, wherein

said organic protecting film has a linear expansion coefficient equivalent to the linear expansion coefficient of said stress relaxing layer.

5. (Original) A semiconductor device as claimed in claim 3, wherein said stress relaxing layer is composed of porous polytetrafluoroethylene.

6. (Original) A semiconductor device as claimed in claim 3, wherein said conductive portion in said via-hole is composed of conductive resin.

7. (Cancelled).

8. (Cancelled)

9. (Currently Amended) A semiconductor device comprising:

a semiconductor chip,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes of said semiconductor chip are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer,

anisotropic conductive material for connecting electrically said circuit layer and said electrodes on said semiconductor chip,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane opposite to the plane, where the circuits and electrodes of said semiconductor chip are formed, wherein

said porous stress relaxing layer has a greater porosity than that of the organic protecting film, and

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed to outside of said semiconductor device on a same plane.

10. (Currently Amended) A semiconductor wafer comprising:

a chip for forming a semiconductor device, having a plurality of chip areas comprising circuits and electrodes, respectively,

a porous stress relaxing layer provided on a plane of said chip, whereon the circuits and the electrodes are formed,

a circuit layer provided on said stress relaxing layer, and connected to said electrodes, and

external terminals provided on said circuit layer, wherein

an organic protecting film is provided on the plane opposite to the plane, whereon said porous stress relaxing layer is provided, of said chip,

said porous stress relaxing layer has a greater porosity than that of the organic protecting film, and

side planes of the stress relaxing layer are exposed to outside of the semiconductor device.

11. (Currently Amended) A semiconductor wafer comprising:

a chip for forming a semiconductor device, having a plurality of chip areas comprising circuits and electrodes, respectively,

a porous stress relaxing layer provided on a plane of said chip, whereon the

circuits and the electrodes of said chip area are formed,

a circuit layer provided on said stress relaxing layer,

via-holes provided between said electrodes and said circuit layer,

conductive portions for electrically connecting said circuit layer and said electrodes in said via-holes,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane, opposite to the stress relaxing layer, of said chip,

wherein said porous stress relaxing layer has a greater porosity than that of the organic protecting film, and

wherein side planes of the stress relaxing layer are exposed to outside of the semiconductor device.

12. (Previously Presented) A semiconductor wafer as claimed in any one of claims 10 and 11, wherein

said organic protecting film has a linear expansion coefficient equivalent to the linear expansion coefficient of said stress relaxing layer.

13. (Previously Presented) A semiconductor wafer as claimed in any one of claims 10 and 11, wherein

said stress relaxing layer is composed of porous polytetrafluoroethylene.

14. (Original) A semiconductor wafer as claimed in claim 11, wherein said conductive portion in said via-hole is composed of conducive resin.

15. (Cancelled).

16. (Cancelled).

17. (Currently Amended) A semiconductor wafer comprising:

a chip for forming a semiconductor device, having a plurality of chip areas comprising circuits and electrodes, respectively,

a porous stress relaxing layer provided on a plane of said chip, whereon the circuits and the electrodes of said chip area are formed,

a circuit layer provided on said stress relaxing layer,

anisotropic conductive material for connecting electrically electrodes on a chip and a circuit layer,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane opposite to the plane, whereon said circuits and electrodes are formed, of said chip,

wherein said porous stress relaxing layer has a greater porosity than that of the organic protecting film, and

wherein side planes of the stress relaxing layer are exposed to outside of the semiconductor device.

18. (Currently Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming a stress relaxing layer on a plane, whereon circuits and electrodes of respective chip areas are formed, of a semiconductor wafer,

forming an organic protecting film on the plane of said semiconductor wafer opposite to the plane where the electrodes of said respective chip areas are formed,

wherein said porous stress relaxing layer has a greater porosity than that of the organic protecting film,

forming via-holes in said stress relaxing layer on said chip areas,

forming conductive portions in said via-holes,

forming circuits on said stress relaxing layer,

forming external terminals on said circuit layer, and

cutting said chip areas, the substrate comprising said circuits, and said organic protecting film along a same plane so that a semiconductor device obtained by the cutting becomes a minimum operation unit.

19. (Currently Amended) A method [[for]] of manufacturing a semiconductor device comprising the steps of:

forming a circuit layer on a porous stress relaxing layer,

adhering said stress relaxing layer comprising the circuit layer to a plane, whereon electrodes are formed, of a chip area,

forming an organic protecting film [[to]] on a plane opposite to the plane comprising said chip area, wherein said porous stress relaxing layer has a greater

porosity than that of the organic protecting film,

forming via-holes in said stress relaxing layer,

forming [[a]] conductive portions in said via-hole,

forming external terminals on said circuit layer; and

cutting said chip areas, the substrate comprising said circuits, and said organic protecting film along a same plane so that [[the]] a semiconductor device obtained by the cutting becomes a minimum operation unit.

20. (Previously Presented) A semiconductor module mounted with plurality of semiconductor devices as claimed in any one of claims 2 to 6 and 9.

21. (Previously Presented) A semiconductor device as claimed in any one of claims 2, 3 and 9, wherein said side planes of the stress relaxing layer, the semiconductor chip and the organic protecting film respectively form peripheral edges of the stress relaxing layer, the semiconductor chip and the organic protecting film.

22. (Previously Presented) A semiconductor wafer as claimed in any one of claims 10, 11 and 17, wherein said side plane of the stress relaxing layer forms a peripheral edge thereof.

23. (Previously Presented) A semiconductor device as claimed in any one of claims 2, 3 and 9, wherein said stress relaxing layer is adhered to the semiconductor chip by an adhesion layer, and a linear expansion coefficient of the organic protecting

film is substantially equivalent to the linear expansion coefficient of said adhesion layer.

24. (Previously Presented) A semiconductor device as claimed in claim 4, wherein said stress relaxing layer is adhered to the semiconductor chip by an adhesion layer, and a linear expansion coefficient of the organic protecting film is substantially equivalent to the linear expansion coefficient of said adhesion layer.

25. (Cancelled).

26. (Previously Presented) A semiconductor device as claimed in any one of claims 2, 3 and 9, wherein the organic protecting film is colored black.

27. (Previously Presented) A semiconductor device as claimed in any one of claims 2, 3, 9, 10, 11 and 17, wherein the porous stress relaxing layer has a breathing property.

28. (Previously Presented) A semiconductor device as claimed in any one of claims 2, 3, 9, 10, 11 and 17, wherein said porous stress relaxing layer is made of a material selected from the group consisting of polycarbonate, polyester, polytetrafluoroethylene, polyethylene, polypropylene, polyvinylidene fluoride, cellulose acetate, polysulfone, polyacrylonitrile, polyamide and polyimide.